REMARKS

The Official Action mailed January 18, 2002 has been received and its contents carefully noted. Filed herewith is a *Petition for One Month Extension of Time*, which extends the period for response to May 18, 2002. Thus, it is respectfully submitted that this response is timely filed.

Claims 1-20 are pending in the present application. Claims 1, 3-6, 8-11, 13-16, and 18-20 have been amended and claims 1, 6, 11 and 16 are independent. For the reasons set forth in detail below, claims 1-25 are believed to be in condition for allowance and favorable reconsideration is requested.

Initially, the Applicants have amended the specification to correct the minor matters of form noted by the Examiner and to correct other typographical matters noted by applicant.

The Office Action next rejects claims 3, 8, 13 and 18 under 35 U.S.C. §112 first and second paragraphs, asserting that the "shift register circuit over said substrate" is of unclear scope and does not appear to have support in the specification and lacks antecedent basis. In response, the Applicants have amended the claims to delete the term "over said substrate" and have amended the specification to correct several instances of "shift resistor" to "shift register." No new matter is added by these amendments and it is respectfully submitted that the features of the claims are clear in scope, supported by the specification and positively recited. The amendments are merely clarifying in nature, and should not in any way affect the scope of protection afforded the claims for infringement purposes, particularly, under the Doctrine of Equivalents.

The Official Action next rejects claims 5 and 10 based on double patenting of the non-statutory type over the claims of U.S. Patent No. 6,194,740 to Zhang, which issued from the parent application, considered together with Yamamoto. The Applicants respectfully traverse the Examiner's rejection. Independent claims 1 and 6 are believed to be distinguished from Yamamoto as discussed in more detail below, and the Applicants respectfully submit that dependent claims 5 and 10 are patentably distinct

from Zhang because the claimed features are not included in Zhang's claims. Reconsideration is requested.

The Office Action also rejects claims 15 and 20 based on double patenting of the non-statutory type over the claims of Zhang considered together with Morozumi. The Applicants respectfully traverse the Examiner's rejection. As above, corresponding independent claims 11 and 16 are distinguished from Morozumi, and the Applicants respectfully submit that dependent claims 15 and 20 are patentably distinct from Zhang because the claimed features are not included in Zhang's claims. Reconsideration is requested.

The Office Action next rejects claims 1, 2, 4, 6, 7 and 9 as anticipated by U.S. Patent No. 5,216,491 to Yamamoto. The Applicants respectfully traverse the Examiner's rejection. Yamamoto does not teach or suggest all the elements of the independent claims as amended, either explicitly or inherently.

Independent claims 1 and 6 recite circuit structures shown in Fig. 3 of the present application, which denotes a linear image sensor and is described in Embodiment 8 of the specification. Amended independent claims 1 and 6 further recite a capacitor electrically connected to the optical sensor between the thin film transistor and the optical sensor, wherein a second electrode of the capacitor is at a ground potential. This feature is supported by reference numeral 3002 in Fig. 3. On the other hand, although Yamamoto may teach a capacitor electrically connected to the optical sensor between the thin film transistor and the optical sensor, Yamamoto fails to teach that a second electrode of the capacitor is at a ground potential.

For the reasons stated above, reconsideration and withdrawal of the rejection of independent claims 1 and 6 under 35 U.S.C. § 102 is in order and respectfully requested. Likewise, it is believed that dependent claims 2, 4, 7 and 9 are likewise allowable in that they depend from what is believed to be allowable base claims 1 and 6.

The Official Action next rejects claims 3 and 8 as obvious based on the combination of Yamamoto and U.S. Patent No. 4,549,088 to Ozawa. The Applicants respectfully traverse the Examiner's rejection because the Examiner has not made a

prima facie case of obviousness. As claims 3 and 8 depend from claims 1 and 6, respectively, please incorporate the arguments above with respect to the deficiencies in Yamamoto. Ozawa does not cure the deficiencies in Yamamoto. Reconsideration of the rejection of claims 3 and 8 is respectfully requested.

The Official Action further rejects claims 11-14 and 16-19 as anticipated by U.S. Patent No. 4,862,237 to Morozumi, and rejects claims 11-20 as anticipated by U.S. Patent No. 5,200,634 to Tsukuda. The Applicants respectfully traverse the Examiner's rejections. Morozumi and Tsukuda do not teach or suggest all the elements of the independent claims, either explicitly or inherently.

Independent claim 11 recites a circuit structure shown in Fig. 4, which denotes an area image sensor and is described in Embodiment 9 of the specification. Amended independent claim 11 recites that a fourth electrode of the optical sensor is electrically connected to a bias terminal, which is supported by reference numeral 4007 in Fig. 4. Similarly, claim 16 also recites a circuit structure shown in Fig. 4. Amended independent claim 16 also recites that the fourth electrode of the optical sensor is electrically connected to a bias terminal, and a capacitor is electrically connected to the bias terminal, which are supported in Fig. 4.

Morozumi and Tsukuda, however, fail to teach the above features, explicitly or inherently. Therefore, since the prior art fails to disclose each and every feature recited in the claims. It is respectfully submitted that the claims cannot be anticipated thereby and reconsideration is requested. Likewise, it is believed that dependent claims 12-15 and 17-20 are likewise allowable in that they depend from what is believed to be allowable base claims 11 and 16.

The Office Action also rejects claims 5 and 10 as obvious based on the combination of Yamamoto and Tsukada. The Applicants respectfully traverse the Examiner's rejection because the Examiner has not made a *prima facie* case of obviousness. As claims 5 and 10 depend from claims 1 and 6, respectively, please incorporate the arguments above with respect to the deficiencies in Yamamoto. Tsukada does not cure the deficiencies in Yamamoto and thus reconsideration of the rejection of claims 5 and 10 is respectfully requested.

The Official Action further rejects claims 16-20 as obvious based on the combination of Tsukada and Morozumi. The Applicants respectfully traverse the Examiner's rejection because the Examiner has not made a *prima facie* case of obviousness. With respect to independent claim 16, please incorporate the arguments above with respect to the deficiencies in Tsukada. Morozumi does not cure the deficiencies in Tsukada. Reconsideration of the rejection of claims 16-20 is respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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MARKED-UP VERSION OF THE SPECIFICATION

Before the first sentence of the specification, amend the sentence as follows:

This application is a Divisional of Application Serial No. 09/115,840 filed July 15, 1998, now U.S. Patent No. 6,194,740.

On Page 6, Second Full Paragraph

The amorphous silicon layer is formed in contact with the drain and channel forming region. The depletion layer is formed between the drain and channel forming region. Since the amorphous silicon is in contact with the drain and channel formation region, the depletion layer can be formed from the drain through the inside of the amorphous silicon layer. The amorphous silicon layer allows the depletion layer extending from the drain to be formed therein when the drain voltage is applied, to transmit [phtocarriers] photocarriers produced in the amorphous silicon layer to the channel forming region immediately after the production by the depletion layer

On Page 12, Fourth Full Paragraph continuing onto Page 13, through the First Full Paragraph:

A Fermi level is not necessarily located at the band gap center when forming amorphous silicon. Rather, the Fermi level shifts in a direction to form a pseudo n-type semiconductor despite no doping due to its structural problem. When the amorphous silicon is doped with p-type [dopnats] dopants such as boron of 3 Group and the like at $5x10^{16}$ to $1x10^{18}$ cm^{-3}, the Fermi level can be set at the band center. The resulting amorphous silicon layer, although doped with dopants, since the location of the Fermi level is closer to an intrinsic state than that of the non-dope silicon, is considered as a substantially intrinsic state.

A transparent conductive film 1009 is formed on the amorphous silicon layer 1008. Indium tin oxide (ITO), tin oxide, and the like may be used for the film 1009. The transparent conductive film 1009 is used for application of a voltage between the source region 1007 and the film. In the present embodiment, the transparent conductive film 1009 utilizes ITO. ITO having a thickness of 1000 to 2000 Å is used considering its transmission ratio and electrical resistance value. Typically, ITO with a thickness of 1200 Å is used. ITO is material to form a Schottky junction by coupling to the amorphous silicon layer, which results in a depletion layer formed from the junction surface through the inside of the amorphous silicon layer as deep as 1000 to 3000 Å approximately by the [schottky] Schottky barrier.

On Page 20, Second and Third Full Paragraphs

Holding [capacity] capacitor 3002 for holding electrical charges produced by photo carriers collected into a source may be separately provided or may be substituted by TFT parasitic [capacity] capacitance. In the present embodiment, the holding [capacity] capacitor is separately disposed. A switch TFT 3001 is used as a switch to transfer electrical charges accumulated in the holding holding [capacity] capacitor to [capacity] capacitor 3003. The gate of the switch TFT 3001 is coupled with a shift [resistor] register for sequential application of a voltage to the shift [resistor] register in synchronization with a clock.

Electrical charges in the capacity 3003 are output into an output 3006 as electrical signals through an amplifier 3005. A reset TFT 3004 is disposed between the [capacity] capacitor 3003 and a ground for resetting the capacitor 3003.

On Page 21, First Full Paragraph continuing through Third Full Paragraph.

Holding [capacity] capacitor 4002 for holding electrical charges produced by photo carriers collected into a source may be separately disposed or may be substituted by TFT parasitic [capacity] capacitance. Providing the [capacity] capacitor separately is

more preferable. A switch TFT 4001 is used as a switch to transfer electrical charges accumulated in the holding [capacity] capacitor to [capacity] capacitor 4002. The gate of the switch TFT 4001 is coupled with a vertical shift [resistor] register 4011, and the source or drain is coupled with a horizontal shift [resistor] register 4010 through an analog switch 4009. A voltage is sequentially applied to each shift [resistor] register in synchronization with a clock.

Signals transmitted through the analog switch 4009 are output into an output 4006. For a scanning method, an optical signal in the first column is output by sequentially applying a [voltageto] voltage to the horizontal shift [resistor] register from the first to the last column while applying a voltage to the first row of the vertical shift [resistor] register. Next, an optical signal in the second column is output by sequentially applying a voltage to the horizontal shift [resistor] register from the first to the last column while applying a voltage to the second row of the vertical shift [resistor] register. Repeating this process until the last row of the vertical shift [resistor] register is applied with a voltage completes sensing of one screen.

MARKED-UP VERSION OF THE AMENDED CLAIMS

1. (Amended) An image sensor comprising:

[a plurality of optical sensors arranged in a linear form;

a plurality of thin film transistors, a first electrode of each of said thin film transistors being electrically connected to each of said optical sensors in series;

a plurality of amplifiers, each of said amplifiers being electrically connected to a second electrode of said each of said thin film transistors]

an optical sensor formed over a substrate;

a thin film transistor electrically connected to said optical sensor in series; and

a capacitor having a first electrode and a second electrode, wherein said first electrode is electrically connected to said optical sensor between said optical sensor and said thin film transistor, and wherein said second electrode is at a ground potential.

3. (Amended) An image sensor of claim 1 wherein a gate electrode of said [each of said] thin film [transistors are] transistor is electrically connected to [at] a shift register circuit [over said substrate].

4. (Amended) An image sensor of claim 1 wherein said [second electrode of said each of said] thin film [transistors are] transistor is electrically connected to a signal output terminal.

5. (Amended) An image sensor of claim 1 wherein said optical sensor [comprising] comprises an amorphous semiconductor layer formed over a bottom gate type thin film transistor.

6. (Amended) An image sensor comprising:

[a plurality of optical sensors arranged in a linear form;

a plurality of thin film transistors electrically connected to capacitors, a first electrode of each of said thin film transistors being electrically connected to each of said

optical sensors in series, and said capacitors being electrically connected to said optical sensors in parallel;

a plurality of amplifiers electrically connected to a second electrode of said each of said thin film transistors]

an optical sensor formed over a substrate;

a thin film transistor electrically connected to said optical sensor in series;

a capacitor having a first electrode and a second electrode, wherein said first electrode is connected to said optical sensor between said optical sensor and said thin film transistor, and wherein said second electrode is at a ground potential ; and

an amplifier electrically connected to said thin film transistor in series.

8. (Amended) An image sensor of claim 6 wherein a gate electrode of said [each of said] thin film [transistors are] transistor is electrically connected to at least one shift register circuit [over said substrate].

9. (Amended) An image sensor of claim 6 wherein said [second electrode of said each of said thin film transistors are] amplifier is electrically connected to a signal output terminal.

10. (Amended) An image sensor of claim 6 wherein said optical sensor [comprising] comprises an amorphous semiconductor layer formed over a bottom gate type thin film transistor.

11. (Amended) An image sensor comprising:

a plurality of row lines and a plurality of column lines arranged in a matrix form over a substrate;

a plurality of thin film transistors formed over said substrate, a gate electrode of each of said thin film transistors being electrically connected to at least one of said

a plurality of capacitors, each of said plurality of capacitors being electrically connected to said second electrode and said bias terminal, and being electrically connected to each of said plurality of optical sensors in parallel.

18. (Amended) An image sensor of claim 16 wherein said plurality of row lines and said plurality of column lines are electrically connected to shift register circuits [over said substrate].

19. (Amended) An image sensor of claim 16 wherein each of said [second electrodes] plurality of column lines is electrically connected to a signal output terminal.

20. (Amended) An image sensor of claim 16 wherein said optical sensor [comprising] comprises an amorphous semiconductor layer formed over a bottom gate type thin film transistor.